# How I Learned to Stop Worrying and Love Physical Design

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## ABSTRACT

Silicon prototypes (tapeouts) are crucial in realizing new hardware accelerator designs, yet physical design continues to be a formidable bottleneck which prevents more designs from reaching tapeout. We explore some possible factors behind the difficulty and speculate on some paths forward.

## 1 INTRODUCTION

Silicon prototypes (or tapeouts) play a crucial role in the development and evaluation of new hardware accelerator architectures. These prototypes validate architectural assumptions and decisions with the highest fidelity performance and power results [36]. This is particularly important as some architectural limitations might only surface during physical design when issues such as congestion, routability, and design violations arise [29].

Agile hardware design is a highly promising approach for addressing the challenges of hardware design. It is an adaptation of agile software development centred around regular cycles which run through all the phases of hardware design, culminating in a tape-in[1] that reflects all stages of the hardware design process [24]. This approach takes advantage of tool-focused advances such as [6][4] to enable small teams to more efficiently deliver a design ready for tapeout. [24] is a successfully applied example of agile hardware design which has produced numerous experimental RISC-V silicon prototypes [4].

However, physical design remains a major bottleneck in agile hardware design. Having one step take much much longer than other steps in the process throws agile off-balance - agile tape-ins become increasingly bottlenecked on the physical design before collapsing to a waterfall-like phase in the last few weeks before tapeout as all efforts become focused on physical design [37][27]. This issue greatly impedes the progress of hardware accelerator development as many new proposals do not make it to silicon due to the long and intensive process of physical design. As a result, the critical bottleneck of physical design continues to hinder the advancement of hardware design and prevents the production of high-fidelity results to guide future architectural research.

## 2 WHY IS PHYSICAL DESIGN SO CHALLENGING?

### 2.1 Factor 1: classical physical design flows are deficient

Classical physical design flows[2] (see Figure 1) suggest that designing a usable physical layout is a merely matter of running some tools once with straightforward parameters [37]. This simplistic view, however, fails to take into account the many complexities involved in this process. A slightly more representative flow is shown in Figure 2. Furthermore, typical flows intermix distinct information about the design, the physical implementation, the CAD tool, and the PDK,[3] making physical design re-use difficult. Additionally, typical flows do not empower the user to iteratively run tools multiple times in order to get a correct layout [37]. These factors result in a painful experience of even starting to use physical design tools in a project.

### 2.2 Factor 2: place-and-route is algorithmically hard

Place-and-route is considered to be an NP-hard problem [21] [35]. While NP-complete problems can be found in software compilation, often the NP-completeness in those problems can be avoided in practice. For example, while register allocation is frequently posed as an NP-complete problem, its classical analysis yields NP-completeness if and only if no spilling [4] are allowed [10]. In practice, many compilers do not aim for spill-free compilations [30], greatly reducing the computational complexity of the problem while still providing a functional compilation output.

However, this difficulty cannot be easily avoided in place-and-route, as violations will result in unmanufacturable or non-functional circuits. A mismatch of expectation materialises when place-and-route tools are advertised as "compilers"[5]; we expect them to provide usable (if not sub-optimal) outputs that do not require manual intervention [37][27]. The analogy in software would be needing to manually fix assembly generated after running gcc/clang. In short, there is unlikely to be a "silver bullet" in physical design. [37].

[1] A tape-in is an intermediate-stage fabricatable design that may be missing features. It is the hardware analogue of an agile software release, designed to encourage responsive, continuous development style over large monolithic leaps [24].

[2] Also referred to as "VLSI flows".

[3] Process design kit: a set of technical information provided by a semiconductor foundry to enable designers to target a particular manufacturing process.

[4] And no control flow graph modifications either.

[5] e.g. IC Compiler

*LATTE '24, April 27, 2024, San Diego, CA, USA*

**Figure 1: An "advertised" VLSI flow [37][27]**

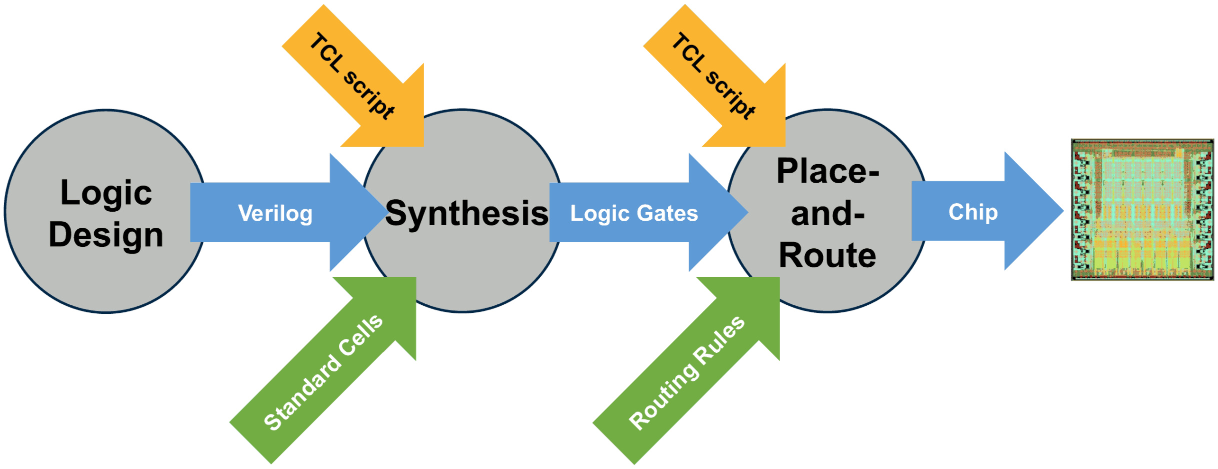
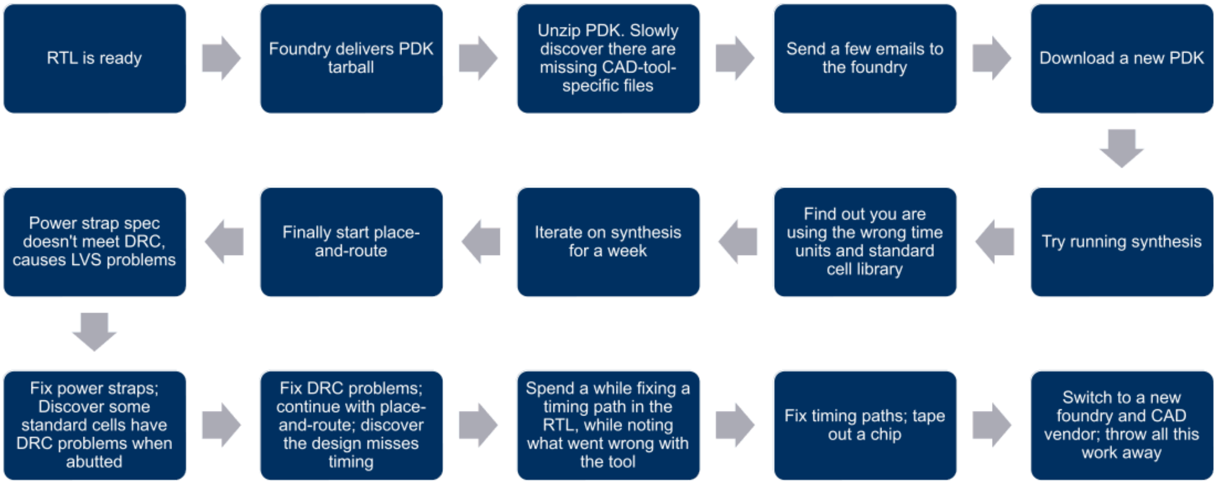


**Figure 2: A more realistic (yet still simplified) VLSI flow [37][27]**


RTL is ready
Foundry delivers PDK tarball
Unzip PDK. Slowly discover there are missing CAD-tool-specific files
Send a few emails to the foundry
Download a new PDK
Try running synthesis
Find out you are using the wrong time units and standard cell library
Iterate on synthesis for a week
Finally start place-and-route
Power strap spec doesn't meet DRC, causes LVS problems
Fix power straps; Discover some standard cells have DRC problems when abutted
Fix DRC problems; continue with place-and-route; discover the design misses timing
Spend a while fixing a timing path in the RTL, while noting what went wrong with the tool
Fix timing paths; tape out a chip
Switch to a new foundry and CAD vendor; throw all this work away

### 2.3 Factor 3: dominant approaches are not correct-by-construction

Many current place-and-route algorithmic approaches are primarily heuristic/statistical-based in order to address performance challenges [18]. [6] These approaches work by converging on increasingly correct results through iterative means or randomness. However, due to the non-convex nature of NP-hard problems [17], these methods cannot guarantee a correct layout, leaving room for potential errors/violations.

Finally, even specialized place-and-route algorithms often make sacrifices to address performance challenges, leaving violations in the final layout [34][12]. This situation is both time-consuming and frustrating for hardware designers, as they are often forced to spend a significant amount of time and effort fixing these violations manually [37][27][8][31].

### 2.4 Factor 4: software engineering methodologies for CAD are limited

Despite the importance of CAD such as place-and-route in hardware design, the current state of CAD software engineering presents several challenges and limitations. A major challenge is that place-and-route CAD tools are typically developed using performance-engineered C/C++ (e.g. [19]). While these languages are chosen for their ability to deliver high performance, it has been shown that they can be difficult to maintain, optimize, and verify [32][25]. [7] This can lead to an increase in security vulnerabilities in often-complex CAD software, as exemplified by [5]. This highlights a need for exploring alternative approaches to address these challenges and mitigate the potential for security vulnerabilities.

[6] Statistical approaches include simulated annealing and spreading; iterative approaches include legalization, rip-up-and-replace [18].

[7] Additionally, the closed-source nature of some popular CAD tools and the economics of chip design may also play a role.

## 3 THE WAY FORWARD?

We present a few viewpoints from which to view the current physical design tooling situation.

The first viewpoint maintains that the current state of place-and-route in physical design is sufficient. It also means that realizing silicon prototypes will by and large remain inaccessible to most (small teams of) designers. Physical designers would continue to be hindered by needing to manually fix design violations generated by tools.[8] Additionally, the challenges associated with current tooling create a disincentive for new engineers and researchers to enter hardware design, leading to an uncertain future for the field as a whole [15]. Finally, this creates a disincentive as upstream advancements can become bottlenecked in physical design, leaving the road to agile hardware design incomplete.

The second viewpoint suggests to invest into better system-level tools. Tools such as Hammer [37][27] address many systems-level challenges. Other approaches include FuseSoC/Edalize [20] and Mflowgen [11] among others. Chipyard integrates the above work into an architectural/RTL-level generator [3]. While these projects help lower the barrier for physical design, they do not address deficiencies and issues with the underlying tools. Additionally, they are unable to provide significant insight into the internal workings of CAD tools, limiting opportunities for further research.

The third viewpoint is to invest into underlying open source tools. For example, OpenROAD [1] has made signficant inroads towards a complete and usable open source flow similar to ICC or Innovus. This would be an essential piece of infrastructure for open source tools that would also greatly lower the barrier for entering into physical design, especially if integrated with system-level tools. Challenges include, if viewed from merely the open source angle without incorporating novel methodologies, lack of ecosystem investment, high expectations, security and correctness concerns [1].

A fourth viewpoint looks for alternative methodologies instead of traditional place-and-route techniques. One popular approach is to forgo place-and-route entirely and instead use expert insight to write scripts or tools to generate layouts. This approach has been adopted in projects such as [13][16]. However, these systems are very time-consuming to use and do not guarantee correctness. More automated tools could open opportunities for co-optimization that can be missed by hand-written layout systems.

Another alternative methodology would be to leverage formal methods. Given the explosion in design complexity and rules, it has become increasingly difficult to ensure that correctness rules are met in conjunction with the increased demands on PPA[9] [26]. Despite the impressive recent advances in AI/ML, significant concerns remain around reliability and trustworthiness which pose verification challenges [23]. While formal methods have been known for poor performance compared to traditional algorithm-based approaches, recent advances in SMT solving have been pushing the frontier [7][14]. They have shown promise in other domains including web layout engines [28], dungeon generation [38], and automotive plant layouts [9] which serves as a source of inspiration.

[8] For example: references to all-nighters in [22][2][33]

[9] "Power, performance, area" is a shorthand for evaluation metrics for hardware designs.

## 4 ACKNOWLEDGEMENTS

The authors would like to thank Richard Lin for his review and input on the manuscript.

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