Language-based Hardware Communication Safety and Liveness

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ABSTRACT

Emerging hardware description languages (HDLs) provide new type annotations to abstract from low-level details [3, 9, 11, 12, 15], enabling opportunities for modular and scalable structural verification at design stage. However, verification of behavioural properties among communicating hardware modules—such as ensuring liveness and communication safety—remain largely unsupported in modern HDLs. In this paper, we present **Pact**, a language extending a recent HDL called Anvil [14] with a novel session type-based system. Our proposed type system explicitly models synchronous clock cycles and introducing new type constructs to capture communication contracts between hardware modules. It offers abstractions to reason about liveness and communication safety between hardware components. Additionally, we give a sound and complete algorithm for verifying them statically. *Our evaluation shows that our type abstractions offer a factor of 2^{70} to 2^{270} in state space reduction over that of concrete RTL designs, when verifying* 10 *real hardware designs.*

1 INTRODUCTION

Hardware designs typically consist of numerous concurrent modules that communicate with one another. In such communication, a sender shares a value with a receiver in a particular clock cycle. Two properties are highly desirable: (1) *communication safety*—the time the sender intends to send the value and the time the receiver intends to receive the value are synchronized; (2) *liveness*—all hardware modules eventually make progress, and in particular, do not deadlock for message communication.

Traditionally, such properties are verified post design through testing or model checking, which suffers from unsoundness and state explosion. While recent research has started investigating language-based approaches that allow sound design-time hardware verification, the properties studied so far have been limited to local low-level properties surrounding wire and register use, such as timing safety, combinational loop freedom, structural hazard freedom, and so on. Verifying communication safety and liveness, however, requires reasoning about the overall behaviour of modules. In this work, we aim to fill in this gap and propose a language-based approach for verifying communication safety and liveness in hardware. The result of our effort is Pact, a hardware description language (HDL) with a type system for verifying such properties.

A natural option is to introduce multiparty session types, which have been used to verify similar properties for software systems, to HDLs. Session types capture relevant behaviour of communication participants. When a collection of session types are compatible, they guarantee communication safety and deadlock freedom. However, adapting session types is not straightforward due to a fundamental mismatch between existing session type abstractions and the execution model of synchronous digital hardware. Specifically, such a mismatch requires us to overcome three main challenges: (1) Existing session types [4, 7, 8] typically abstract away cycle-level timing hardware communication; (2) They restrict internal and external choice structures, limiting the expressiveness for communication patterns common to hardware designs; (3) Prior approaches to session types define compatibility syntactically [1, 5] or compromise modularity [2, 10], which is essential for hardware design.

Our work, Pact, addresses these challenges first by extending session types with modelling for synchronous hardware behaviour such as synchronous latency and unrestricted multiparty choice. We then devise an automata-based type compatibility algorithm that is sound and complete, overcoming the limitations of existing type compatibility formulations. We implement Pact as an extension to Anvil [14], and evaluate its effectiveness. Our experiments across 10 real-world hardware designs show that compared to concrete register-transfer-level (RTL) designs, Pact achieves a state space reduction by a factor of 2^{70} to 2^{270} across different types of designs. We intend to open-source Pact and potentially merge it into the upstream Anvil once the development has matured.

$$e ::= x \mid v \mid e \ \texttt{bop}\ e \qquad v ::= \texttt{true} \mid \texttt{false} \qquad B ::= \emptyset \mid B, \hat{a} : P$$
$$a ::= \texttt{send}\ m\ e \mid x = \texttt{recv}\ m\ \texttt{in}\ P \qquad \hat{a} ::= \texttt{send}\ m\ e \mid x = \texttt{recv}\ m$$
$$P ::= \texttt{skip} \mid a \mid X \mid \texttt{cycle} \mid \texttt{end}_t \mid P \parallel P \mid P; P \mid \texttt{let}\ x = e\ \texttt{in}\ P$$
$$\mid \texttt{if}\ e\ \texttt{then}\ P\ \texttt{else}\ P \mid \texttt{fair-if}_\eta\ e\ \texttt{then}\ P\ \texttt{else}\ P$$
$$\mid \texttt{offer}\ B\ \texttt{else}\ P \mid \texttt{xoffer}\ B\ \texttt{else}\ P \mid \mu X.P$$

Figure 1: Abstract syntax of processes in Pact.

2 PACT

Following Anvil [14], Pact models hardware modules as *processes* which communicate by passing messages across *channels*. Such *message passing* is the only way for processes to communicate.

2.1 Processes

2.1.1 Syntax. Figure 1 presents the abstract syntax of Pact processes. In addition to the basic primitives cycle and message passing primitives in Anvil, Pact includes explicit constructs for more expressive communication patterns, particularly for multiparty external choice, and for expressing safety specification.

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The exclusive (`xoffer`) and non-exclusive (`offer`) constructs both default to $P_{\texttt{else}}$ if no messages in B can be exchanged. However, if multiple matches exist, `xoffer` non-deterministically executes one, while `offer` executes all in parallel. These unique constructs enable external choices dependent on multiple parties.

Some lightweight constructs help specify aspects of the desired safety properties. For example, consider the branching construct ($\texttt{fair-if}_\eta\ e\ \texttt{then}\ P_1\ \texttt{else}\ P_2$) that is *assumed* to be fair, i.e., either neither or both of P_1 and P_2 are executed infinite times. Here, the identifier η allows us to track which branching construct each branching decision corresponds to in the semantics. Likewise, $\texttt{end}_t$ is used to specify a state of interest, which when reached demarcates progress in the process identified by t. In Pact, the RTL design consists of a set of looping processes $P_1, P_2, \cdots, P_n$ provided by the designer. Our safety specification requires that all processes perform infinitely many loop iterations. Therefore, Pact designs are expected to be structured as

$$\mu X.(P_1; \texttt{end}_1; X) \parallel \mu X.(P_2; \texttt{end}_2; X) \parallel \ldots \parallel \mu X.(P_n; \texttt{end}_n; X).$$

2.1.2 Semantics. The semantics of Pact processes is defined using a labelled transition system (LTS) (S, Σ, T), where each transition label $\sigma \in \Sigma$ represents an *action*:

$$\sigma ::= m\checkmark \mid \# \mid \$_t \mid \texttt{true}_\eta \mid \texttt{false}_\eta.$$

An $m\checkmark$ action represents a message exchange over channel m and # represents elapse of a cycle. A $\$_t$ marks reaching of a state that indicates progress, referred to as a *progress state*, e.g., completion of a process iteration, and $\texttt{true}_\eta$ and $\texttt{false}_\eta$ encode choice decisions.

Each state in S is a process (note that a collect of parallel processes can also be expressed as one process). The run of such an LTS from a state s_0 is a finite/infinite sequence $\rho = (s_0 \xrightarrow{\sigma_0} s_1) \cdot (s_1 \xrightarrow{\sigma_1} s_2) \cdots$ such that for every i, $(s_i \xrightarrow{\sigma_i} s_{i+1}) \in T$. A run is *complete* if it is either infinite or if it terminates in a state s with no outgoing transition.

2.2 Safety

We define safety based on the LTS. Such a definition needs to capture both communication safety and liveness (under specified fairness assumptions). Informally, the definition requires that all complete run of the LTS from a given start state to satisfy either (1) for all (relevant) process identifiers t, $\$_t$ transitions are made infinite times in the run, or (2) for some η, $\texttt{true}_\eta$ or $\texttt{false}_\eta$ transitions are made infinite times, and transitions of the other are made finite times. Note that (1) states progress and (2) states the specified fairness assumptions. Communication safety is implicit: The LTS only allows transitions corresponding to safe communication, and the conditions above imply that the run must be infinite.

2.3 Types

Compared to prior session type formulations, Pact types capture more expressive communication patterns, and use a compatibility checking algorithm that is sound and complete (Section 2.4). The abstract syntax of types is as follows:

$$\begin{aligned}\tau ::= {} & \alpha \mid \$_t \mid \# \mid \texttt{skip} \mid \tau + \tau \mid \tau; \tau \mid \tau \parallel \tau \mid X \mid \mu X.\tau \mid \tau \dot{+}_\eta \tau \\ & \mid \oplus(\tau, \alpha : \tau, \cdots) \mid \wedge(\tau, \alpha : \tau, \cdots) \\ \alpha ::= {} & m! \mid m?\end{aligned}$$

Similar to processes, types include internal choice with fairness assumptions ($\tau \dot{+}_\eta \tau$), exclusive and non-exclusive multiparty external choice ($\oplus(\tau, \alpha : \tau, \cdots)$ and $\wedge(\tau, \alpha : \tau, \cdots)$), as well as the marker for a progress state ($\$_t$).

The satisfiability relation between a type and a process is mostly standard, defined inductively over the syntactic structure. We define the operational semantics of types in the same framework (Section 2.1.2), except that the states are here types instead of processes.

2.4 Type Compatibility

We devise an automata-based sound and complete algorithm for deciding compatibility between types. The high-level idea of the algorithm is straightforward. We start by showing that starting with any type, the set of reachable types in the type semantics is finite (under the restriction that all recursions are at tail positions). This allows us to construct a *finite* LTS which captures the semantics of $\tau_{\text{system}} = \tau_1 \parallel \cdots \parallel \tau_n$. We then observe that the safety properties (Section 2.2) can be encoded as Rabin conditions for ω-automata. This can be achieved through checking for emptiness of the product Rabin automaton. Since types abstract away many irrelevant details in concrete designs, we expect the LTS thus constructed to be smaller in state space. We show this empirically in Section 5.

3 LANGUAGE OVERVIEW

Pact is a language extension to Anvil [14]. We first illustrate the programming model with a simple process description in Anvil:

```
chan arb_worker_ch {
  left req : (logic@#1),
  left done : (logic@#1)
}
proc worker(ep[2] : right arb_w_ch) {
  reg cyc : logic[32];
  loop {
    send ep[0].req(1'd1) >> cycle 1 >>
    if ((*cyc)%3==0) {
      send ep[1].req(1'd1) >> cycle 1 >>
      send ep[0].done(1'd1); send ep[1].done(1'd1)
    } else {
      send ep[0].done(1'd1)
    } >> cycle 1
  } // loop that tracks cycle count (cyc) (skipped for brevity)
}
```

The process `worker` takes two endpoints of channel type `arb_w_ch`. In the channel definition, message labels associated with the `right` endpoint correspond to messages this process receives, while the remaining labels correspond to messages it sends [14].

Operationally, the process first sends a `req` message to the first endpoint and waits one cycle. It then checks whether `cyc` is divisible by three. If so, it sends a `req` message to the second endpoint, waits one cycle, and then sends `done` messages to both endpoints in parallel. Otherwise, it sends a `done` message only to the first endpoint. The loop then repeats after one cycle. Since Pact extends Anvil, every Anvil process is valid in Pact. The behavior of the above process can be checked against the Pact *interface type*:

```
interface worker_itfc(ep[2] : right w_arb_ch) =
  ep[0].req; #1;
  (ep[0].done + (ep[1].req; #1; (#ep[0].done || #ep[1].done))); #1
```

This interface abstracts the communication behavior of the process. It specifies that the process first sends `ep[0].req`, waits one

cycle, and then either sends `ep[0].done` or performs a transaction on the second endpoint consisting of `ep[1].req`, a one-cycle delay, and parallel completion messages on both endpoints. The behavior then repeats after one cycle. All Pact interfaces are implicitly tail-recursive since processes in Anvil/Pact are tail-recursive.

In this syntax, a message identifier such as `ep[0].req` denotes a blocking message exchange and is syntactic sugar for the abstract type[1] $\mu X.\ \oplus(\#; X,\ \texttt{ep[0].req!} : \texttt{skip})$. In contrast, `#ep.req` denotes a non-blocking exchange and corresponds directly to the underlying abstract type, while the remaining operators correspond to constructs of the abstract type language. In Pact, a process may take an instantiation of an interface type as an argument instead of channel endpoints, and the compiler checks that the implementation conforms to the specified interface. It is straightforward to see that the above process conforms to this interface.

Next consider the other endpoint of the channel, implemented by an arbiter that arbitrates between the two workers. Since the arbiter accepts requests from either worker and completes the corresponding transaction, its interface can be written as follows:

```
interface arbiter_itfc(ep[2] : left w_arb_ch) =
  ^(ep[0].req: #1; ep[0].done, ep[1].req: #1; ep[1].done); #1
```

This interface uses the exclusive external choice operator `^` (corresponding to $\oplus$ in the abstract syntax) to indicate that the arbiter will engage in a transaction with exactly one of the endpoints. Intuitively, the arbiter waits until a request arrives from either worker and then completes the corresponding request–done transaction. The program type is syntactic sugar for $\mu X.\ \oplus(\#; X,\ \texttt{ep[0].req?} : \#; \texttt{ep[0].done?},\ \texttt{ep[1].req?} : \#; \texttt{ep[1].done?})$. A Pact implementation that satisfies this type :

```
reg prio : logic; // process signature skipped for brevity
loop {
  xoffer with *prio {
    x = recv ep[0].req => (
      let dn = recv ep[0].done >> set prio := 1'd1
    ),
    ep[1].req => (
      let dn = recv ep[1].done >> set prio := 1'd0
    )
  }
}
```

The `xoffer` construct waits for requests from both endpoints and resolves them via exclusive offer. Pact allows designers to enforce fair arbitration by explicitly specifying priority with `xoffer`. The annotation `with *prio` in the example specifies that the priority between branches is determined by the content of the register `prio`. If such an annotation is omitted, the first branch takes precedence.

Finally, consider a closed system consisting of two workers and two arbiters, where each worker connects to both arbiters and each arbiter connects to both workers. To check compatibility, Pact translates interface types into automata derived from their operational semantics. The synchronous cross-product of these automata exposes a deadlock state in which both workers simultaneously attempt to issue requests to the opposite arbiter while each arbiter waits to complete a transaction with its current endpoint.

[1]Note that we omit the direction (! or ?) of the message passing operation in the concrete syntax as it can be inferred from the endpoint and channel definitions.

Table 1: Comparison of state space: RTL vs type ($\log_2 |N|$)

Component	Participants	RTL State Space	Type State Space	Compatiblity
FIFO	3	81	9.7	✓
Stream FIFO	3	80	8.8	✓
Spill Register	3	70	8.8	✓
RR Arbiter	6	176	18.5	✓
TileLink Crossbar	10	184	34.5	✓
ACE Cache Controller	11	241	39.9	✓
AXI Lite Demux (Read)	8	155	27.4	✓
AXI Lite Demux (Write)	10	144	38.5	✓
AXI Lite Mux (Read)	9	226	33.2	✓
AXI Lite Mux (Write)	11	311	41.7	✓

4 SOUNDNESS

At a high level, we prove soundness—if τ_i satisfies P_i and $\tau_{\text{system}} = \tau_1 \parallel \cdots \parallel \tau_n$ is compatible, then $P_{\text{system}} = P_1 \parallel \cdots \parallel P_n$ is safe—by showing that (1) satisfiability between any τ and P implies that the semantics of P refines that of τ, thus safety of τ transfers to P, and (2) compatibility of τ implies its safety.

5 EVALUATION

We evaluate expressivity using open-source IPs, comparing the state space of our behavioural type models against SystemVerilog implementations (via yosys-abc latch counts). Table 1 demonstrates orders-of-magnitude reductions in state bits ($\log_2 |N|$).

6 DISCUSSION AND FUTURE WORK

We briefly discuss some key aspects of Pact and future directions.

Practicality. For practical convenience, our Pact implementation supports syntactic sugar such as quantification ($\forall$) as a basic form of metaprogramming in the interface types. It also provides type inference, allowing designers to start from a high-level specification and refine it according to the desired behavior.

Real-World Applications. The two main aspects of our work—type satisfiability and type compatibility, are useful in different settings. Type satisfiability is particularly useful when specifying the abstract behavior of a component, such as in type-state programming for drivers [13] which enables formal guarantees at design time for hardware-software co-design. Type compatibility, on the other hand, is useful when complex designs are divided among multiple designers and the overall system must be checked for liveness before implementation. Once the abstract behaviors agree, each designer only needs to ensure that their implementation satisfies the corresponding interface specification. Such a layered approach also opens opportunities for generalizing the method to hybrid session types [6].

Fairness. Although fairness is undecidable in general, it is important for improving the expressivity and scalability of the type system, particularly in cases involving unrestricted or unbalanced choices. Therefore, tractable verification of fairness as a language feature for common cases, such as through verifying monotonicity of priority changes, is an interesting direction for future work.

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